IN THE CLAIMS:

Please amend the claims as follows:

1. (Currently Amended) An integrated circuit package comprising:

a package body;

an integrated circuit die positioned within the package body;

a lead frame including a plurality of leads having portions enclosed within the package body that connect to the integrated circuit die, the plurality of leads having portions enclosed within the package body forming an area; and

an electrically conductive heat sink positioned at least partially within the package body with a surface of a first portion of the heat sink facing the lead frame in close proximity to a substantial part of the enclosed portion of at least eighty percent of the area formed by the plurality of leads of the lead frame having portions enclosed within the package body and with a die-attach area on the surface of the first portion of the heat sink attached to the integrated circuit die, a second portion of the heat sink under the die-attach area and the integrated circuit die projecting away from the first portion of the heat sink ~~under the die-attach area and the integrated circuit die~~, the heat sink coupled to one of a signal voltage and a reference voltage so the heat sink operates respectively as a signal plane and a ground plane for the plurality of leads of the lead frame.

2. (Previously Twice Amended) The integrated circuit package of claim 1, wherein the package body includes one of a transfer molded plastic package body and a preformed ceramic package body.

3. (Previously Twice Amended) The integrated circuit package of claim 1, wherein the integrated circuit die includes one of a Dynamic Random Access Memory integrated circuit die, a Static Random Access Memory integrated circuit die, a Synchronous Dynamic Random Access Memory integrated circuit die, a Sequential Graphics Random Access Memory integrated

circuit die, a flash Electrically Erasable Programmable Read-Only Memory integrated circuit die, and a processor integrated circuit die.

4. (Previously Twice Amended) The integrated circuit package of claim 1, wherein the lead frame includes one of a peripheral-lead finger lead frame, a Leads Over Chip lead frame, and a Leads Under Chip lead frame.

5. (Previously Canceled)

6. (Previously Twice Amended) The integrated circuit package of claim 1, wherein the heat sink is coupled to the reference voltage through one of a wirebond, a conductive adhesive, and a welded connection.

7. (Withdrawn)

8. (Previously Amended) The integrated circuit package of claim 1, wherein the heat sink is positioned only partially within the package body.

9. (Previously Three Times Amended) The integrated circuit package of claim 1, wherein the heat sink is coupled to a printed circuit board outside the package body thereby coupled to one of a signal voltage and a reference voltage.

10. (Previously Amended) The integrated circuit package of claim 8, wherein the second portion of the heat sink projects substantially to one of a top and a bottom of the package body.

11. (Previously Twice Amended) The integrated circuit package of claim 1, wherein the heat sink is positioned within the package body with the surface of its first portion in close

proximity to substantially all of the enclosed portion of each of the plurality of leads of the lead frame.

12. (Previously Amended) The integrated circuit package of claim 1, wherein the heat sink is positioned within the package body with its first portion extending substantially to at least one side of the package body.

13. (Previously Canceled)

14. (Previously Amended) The integrated circuit package of claim 1, wherein the first and second portions of the heat sink are integral with one another.

15. (Previously Amended) The integrated circuit package of claim 1, wherein the first and second portions of the heat sink comprise separate parts.

16. (Previously Amended) The integrated circuit package of claim 1, wherein the heat sink comprises a plurality of parts, each forming a portion of both the first and second portions of the heat sink.

17. (Previously Amended) The integrated circuit package of claim 1, wherein the surface of the first portion of the heat sink includes a recess in which the die-attach area is located.

18. (Previously Amended) The integrated circuit package of claim 1, wherein the heat sink has locking holes therein for locking the heat sink in the integrated circuit package.

19. (Previously Amended) The integrated circuit package of claim 1, further comprising an adhesive attaching the lead frame to the heat sink.

20. (Previously Amended) The integrated circuit package of claim 1, wherein the integrated circuit package comprises one of a Vertical Surface Mount Package, a Small Outline J-lead package, a Thin Small Outline Package, a Quad Flat Pack, and a Thin Quad Flat Package.

21. (Previously Withdrawn)

22. (Currently Amended) An electronic system comprising an input device, an output device, a memory device, and a processor device coupled to the input, output, and memory devices, at least one of the input, output, memory, and processor devices including an integrated circuit package comprising:

a package body;

an integrated circuit die positioned within the package body;

a lead frame including a plurality of leads having portions enclosed within the package body that connect to the integrated circuit die, the plurality of leads having portions enclosed within the package body forming an area; and

an electrically conductive heat sink positioned at least partially within the package body with a surface of a first portion of the heat sink facing the lead frame in close proximity to a substantial part of the enclosed portion of at least eighty percent of the area formed by the plurality of leads of the lead frame having portions enclosed within the package body forming an area and having a die-attach area on the surface of the first portion of the heat sink attached to the integrated circuit die, a second portion of the heat sink ~~being opposite~~ under the die-attach area and the integrated circuit die projecting away from the first portion of the heat sink and the integrated circuit die.

23. (Withdrawn)

24. (Currently Amended) An integrated circuit package comprising:

a package body;

an integrated circuit die positioned within the package body;

a lead frame including a plurality of leads having portions enclosed within the package body that connect to the integrated circuit die, the plurality of leads having portions enclosed within the package body forming an area; and

an electrically conductive heat sink positioned at least partially within the package body with a vertically extending columnar portion surrounded by a horizontally extending skirt portion, said columnar portion having a vertical thickness which is greater than the vertical thickness of said skirt portion, and having a lead frame attachment surface proximate a die-attach surface substantially vertically aligned with the columnar portion, the lead frame attachment surface being attached to the lead frame and extending in close proximity to a substantial part of the enclosed portions of at least eighty percent of the area formed by the plurality of leads of the lead frame having portions enclosed within the package body, the die-attach surface being attached to the integrated circuit die.

25. (Currently Amended) An integrated circuit package comprising:

an integrated circuit die;

a lead frame including a plurality of leads having portions that are connected to the integrated circuit die, the plurality of leads forming an area; and

an electrically conductive heat sink positioned having a surface of a first portion of the heat sink facing the lead frame in close proximity to a substantial part of an enclosed portion of at least eighty percent of the area formed by the plurality of leads of the lead frame and with a die-attach area on the surface of the first portion of the heat sink attached to the integrated circuit die, a second portion of the heat sink under the die-attach area and the integrated circuit die projecting away from the first portion of the heat sink ~~under the die-attach area and the integrated circuit die~~, the heat sink coupled to one of a signal voltage and a reference voltage for the heat sink to operate respectively as a signal plane and a ground plane for the plurality of leads of the lead frame.

26. (Previously Twice Amended) The integrated circuit package of claim 25, further comprising a package body.

27. (Previously Twice Amended) The integrated circuit package of claim 26, wherein the package body includes one of a transfer molded plastic package body and a preformed ceramic package body.

28. (Previously Twice Amended) The integrated circuit package of claim 25, wherein the integrated circuit die includes one of a Dynamic Random Access Memory integrated circuit die, a Static Random Access Memory integrated circuit die, a Synchronous Dynamic Random Access Memory integrated circuit die, a Sequential Graphics Random Access Memory integrated circuit die, a flash Electrically Erasable Programmable Read-Only Memory integrated circuit die, and a processor integrated circuit die.

29. (Previously Twice Amended) The integrated circuit package of claim 25, wherein the lead frame includes one of a peripheral-lead finger lead frame, a Leads Over Chip lead frame, and a Leads Under Chip lead frame.

30. (Previously Canceled)

31. (Previously Twice Amended) The integrated circuit package of claim 25, wherein the heat sink is coupled to the reference voltage through one of a wirebond, a conductive adhesive, and a welded connection.

32. (Withdrawn)

33. (Previously Amended) The integrated circuit package of claim 26, wherein the heat sink is positioned only partially within the package body.

34. (Previously Twice Amended) The integrated circuit package of claim 26, wherein the heat sink is coupled to a printed circuit board outside the package body and is thereby

coupled to one of a signal voltage and a reference voltage so the heat sink operates respectively as a signal plane and a ground plane for the plurality of leads of the lead frame.

35. (Previously Amended) The integrated circuit package of claim 34, wherein the second portion of the heat sink projects substantially to one of a top and a bottom of the package body.

36. (Previously Twice Amended) The integrated circuit package of claim 26, wherein the heat sink is positioned within the package body with the surface of its first portion in close proximity to substantially all of the enclosed portion of each of the plurality of leads of the lead frame.

37. (Previously Amended) The integrated circuit package of claim 26, wherein the heat sink is positioned within the package body with its first portion extending substantially to at least one side of the package body.

38. (Previously Canceled)

39. (Previously Amended) The integrated circuit package of claim 25, wherein the first and second portions of the heat sink are integral with one another.

40. (Previously Amended) The integrated circuit package of claim 25, wherein the first and second portions of the heat sink comprise separate parts.

41. (Previously Amended) The integrated circuit package of claim 25, wherein the heat sink comprises a plurality of parts, each forming a portion of both the first and second portions of the heat sink.

42. (Previously Amended) The integrated circuit package of claim 25, wherein the surface of the first portion of the heat sink includes a recess in which the die-attach area is located.

43. (Previously Amended) The integrated circuit package of claim 25, wherein the heat sink has locking holes therein for locking the heat sink in the integrated circuit package.

44. (Previously Amended) The integrated circuit package of claim 25, further comprising an adhesive attaching the lead frame to the heat sink.

45. (Previously Amended) The integrated circuit package of claim 25, wherein the integrated circuit package comprises one of a Vertical Surface Mount Package, a Small Outline J-lead package, a Thin Small Outline Package, a Quad Flat Pack, and a Thin Quad Flat Pack.

REMARKS

Claims 1 through 4, 6 through 12, 14 through 29, 31 through 37 and 39 through 45 are currently pending in the application.

This amendment is in response to the Final Office Action of July 14, 2003.

Claims 7, 23 and 32 are withdrawn.

Claims 1, 2, 4, 6, 8 through 12, 14 through 20, 24 through 27, 29, 31, 33 through 37 and 39 through 45 are rejected under 35 U.S.C. § 102(b) as being anticipated by Marrs (U.S. Patent 5,701,034) or, in the alternative, under 35 U.S.C. § 103(a) as obvious over Marrs.

Claims 3, 22 and 28 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Marrs as applied to claims 1, 2, 4 through 6, 8 through 20, 24 through 27, 29 through 31 and 33 through 45, and further in combination with Wark (U.S. Patent 5,696,031).

After carefully considering the cited prior art, the rejections, and the Examiner's comments, Applicants have amended claims 1, 22, 24 and 25 such that all remaining claims now clearly distinguish over the cited prior art.

A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Brothers v. Union Oil Co. of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). The identical invention must be shown in as complete detail as is contained in the claim. *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

With respect to the rejection of claims 1, 2, 4, 6, 8 through 12, 14 through 20, 24 through 27, 29, 31, 33 through 37 and 39 through 45 under 35 U.S.C. § 102(b) as being anticipated by Marrs, Applicants respectfully submit that Marrs fails to identically describe each and every element of Applicants' invention as presently claimed to anticipate the presently claimed invention under 35 US.C. § 102. Applicants respectfully submits, similarly to the response to the prior Office Action, that Marrs fails to describe a heat sink with "a second portion" which "[projects] away from the first portion of the heat sink under the die-attach area and the integrated circuit die," as required in claims 1, 22 and 25. While the rejection has been proffered repeatedly, Applicants respectfully submit that the rejection is unsupported. Applicants respectfully request that the Office Action clearly set forth a cite from the reference which

discloses, teaches or suggests a heat sink which is thicker beneath the die attach portion of the packaged semiconductor than at the periphery, as required by the presently amended language of Applicants' claims, and as shown in Applicants Figures 1A, 2A and 3A.

Applicant respectfully suggests that in the Office Action the same reasoning in the above rejection as applied to claim 24 is being applied yet again. The rejection of claim 24 implies that the limitation of a "vertically extending columnar portion surrounded by a horizontally extending skirt portion" is met by heat sinks such as illustrated in Figure 1 or Figure 2A, in which a moat partially defines two portions of the heat sink; one directly under the die, and another extending horizontally away from the die. In order to make it clear that the columnar portion extends further in the downward direction than the skirt portion, Applicants have amended claim 24 to resolve the ambiguity by requiring that the "vertical portion" of the heat sink have a "columnar portion [which has] a vertical thickness which is greater than the vertical thickness of said skirt portion." Page 9, first two paragraphs; Figures 1A, 2A and 3A.

Applicants submit that language in claims 1, 22 and 25 (i.e., "a second portion of the heat sink projecting away from the first portion of the heat sink under the die-attach area and the integrated circuit die") already requires that there be a second portion of the heat sink which is under the first portion, and additionally, extends away from the first portion. The existence of this element is not satisfied by the heat sinks of Figures 1 and 2A. However, in order to remove any doubt as to whether the second portion extends outward or downward from the die, Applicants have simply added to claim 22 (relocated, in claims 1 and 25) the phrase "under the die attach area and the integrated circuit die" so that it clearly modifies "second portion of the heat sink." Applicant submits that the claims as amended clearly disclose a heat sink in which the die-attached portion is bulkier than the peripheral portions. The amendments are amply supported in the specification at page 9 of the Specification, first and second paragraph, as well as figures 1A-C. Applicants respectfully submit that claims 1, 22, 24 and 25 are allowable as amended. Applicants submit that Marrs does not and cannot anticipate the presently claimed invention of claims 1, 2, 4, 6, 8 through 12, 14 through 20, 24 through 27, 29, 31, 33 through 37 and 39 through 45 under 35 U.S.C. § 102 because not all identical elements of the presently claimed invention are identically described in Marrs, either expressly or inherently. Therefore,

claims 1, 2, 4, 6, 8 through 12, 14 through 20, 24 through 27, 29, 31, 33 through 37 and 39 through 45 are allowable over Marrs under 35 U.S.C. § 102.

Applicants further submit that to establish a *prima facie* case of obviousness under 35 U.S.C. § 103 three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Third, the cited prior art reference must teach or suggest all of the claim limitations. Furthermore, the suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on Applicants' disclosure.

With respect to the rejection of claims 1, 2, 4, 6, 8 through 12, 14 through 20, 24 through 27, 29, 31, 33 through 37 and 39 through 45 under 35 U.S.C. § 103 as being obvious over Marrs, Applicants respectfully submits that the cited prior art Marrs reference fails to establish a *prima facie case* of obviousness under 35 U.S.C. § 103 because either Marrs does not teach or suggest Applicants' heat sink element, as set forth above in the presently claimed invention as Marrs does not teach or suggest all the claim limitations of the presently claimed invention.

Thus claims 1, 24 and 25 are allowable, and claims 2, 4, 6, 8 through 12, 14 through 20, 26, 27, 29, 31, 33 through 37and 39 through 45 are allowable as depending from allowable claims.

With respect to the rejection of claims 3, 22 and 28 under 35 U.S.C. § 103(a) as being unpatentable over Marrs as applied to claims 1, 2, 4 through 6, 8 through 20, 24 through 27, 29 through 31 and 33 through 45, and further in combination with Wark (U.S. Patent 5,696,031), Applicant respectfully requests the withdrawal of the rejection for two reasons. First, Applicants respectfully submit that as in the rejections above, all the claim limitations of the presently claimed invention are not taught by Marrs to establish a *prima facie case* of obviousness under 35 U.S.C. § 103. Specifically, Marrs fails to teach or suggest Applicants' presently claimed heat sink. Second, Applicant respectfully submits that Wark is not analogous art, and thus should not be considered as prior art with respect to the application at hand. Wark is a method for stacking different types of chips onto each other. While Wark admittedly considers a Dynamic Random

Access Memory integrated circuit die, a Static Random Access Memory integrated circuit die, a Synchronous Dynamic Random Access Memory integrated circuit die, a Sequential Graphics Random Access Memory integrated circuit die, a Flash Electrically Erasable Programmable Read-Only Memory integrated circuit die, and a processor integrated circuit die as candidates for stacking, Wark teaches none of the other elements of Applicants' claims. The reference does not teach a package body or die inside it, a lead frame, or a heat sink. The Applicants' disclosure is directed at reducing inductive effects on a die due to the lead frame to which it is attached, as well as minimizing heat sink material. See Field of the Invention. In contrast, Wark is relevant to Applicant's device only in that it teaches the stacking of types semiconductor devices which are mentioned in Applicants disclosure. Because Wark has such limited relevance (as underscored by complete lack any elements which would attract the attention of a practitioner who is looking to 1) reduce inductive effects of a lead frame upon the die to which it is attached, and 2) minimize amount of heat sink material), a practitioner is unlikely to search out Wark for any reason to modify Marrs for any reasons. Therefore, any combination of Marrs and Wark fails to a *prima facie case* of obviousness under 35 U.S.C. § 103 for the above reasons. Accordingly, claims 3, 22 and 28 are allowable.

Applicants submit that claims 1, 22, 24 and 25 are allowable, with claims 2 through 4, 6 through 12, 14 through 21, 26 through 29, 31 through 37 and 39 through 45 are allowable as depending from allowable independent claims.

Applicants request the allowance of claims 1 through 4, 6 through 12, 14 through 29, 31 through 37 and 39 through 45 and the case passed for issue.

Respectfully submitted,

James R. Duzan
Registration No. 28,393
Attorney for Applicants
TRASKBRITT
P.O. Box 2550
Salt Lake City, Utah 84110-2550
Telephone: 801-532-1922

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